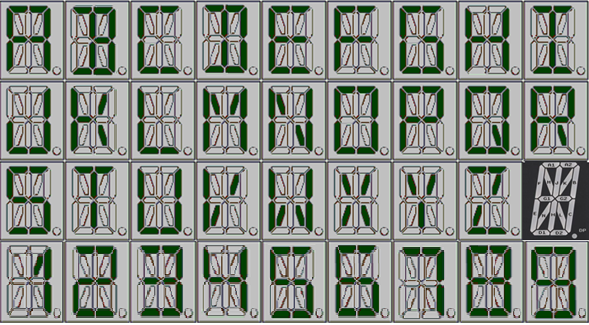
**INSTRUCTIONS.** Design a common anode 16-segment alphanumeric display decoder that shows the text indicated by the professor, there aren’t “Don’t care” values. Complete the table including the missing values, as well as the text of the structural VHDL code and the images of the simulation with all possible cases.



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **A** | **B** | **C** | **D** | **E** | **sA1** | **sA2** | **sB** | **sC** | **sD1** | **sD2** | **sE** | **sF** | **sG1** | **sG2** | **sH** | **sJ** | **sK** | **sL** | **sM** | **sN** | **Hexa** |
| **0** | 2 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **113F** |
| **1** | 1 | 0 | 0 | 0 | 0 | 1 | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** |  |
| **2** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **3** | 2 | 0 | 0 | 0 | 1 | 1 | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** |  |
| **4** | 8 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **5** | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **6** | A | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **7** | B | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |  |
| **8** | C | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **9** | D | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  |
| **10** | E | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **11** | F | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **12** | G | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **13** | H | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **14** | I | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  |
| **15** | J | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **16** | K | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |  |
| **17** | L | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **18** | M | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |  |
| **19** | N | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |  |
| **20** | O | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **21** | P | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **22** | Q | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |  |
| **23** | R | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  |
| **24** | S | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **25** | T | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  |
| **26** | U | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| **27** | V | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |  |
| **28** | W | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |  |
| **29** | X | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |  |
| **30** | Y | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |  |
| **31** | Z | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |  |

|  |  |
| --- | --- |
| **Quartus II Simulation** |  |
|  |  |
| **Structural VHDL Code** | |
|  | |

Fill in the table with the corresponding binary values ​​for each output segment and place the conversion in the "Hexadecimal" column. Deliver this file in PDF format by renaming the file: Group\_Surname\_Name, p. eg: 5C\_Pérez\_Juan to the mail [guillermo.guerrero@upa.edu.mx](mailto:guillermo.guerrero@upa.edu.mx), also send the practice report.

Place in the cell "Simulation in Quartus II", the images of the simulation obtained from printing the screen where each of the possible cases is displayed legibly, grouping the 5 entries in a single entry (shown in unsigned decimal) and grouping all 16 outputs into a single output (displayed in hexadecimal). Shows 4 images legibly, showing in the first image cases from 0 to 7, in the second image cases from 8 to 15, in the third image cases from 16 to 23 and in the last image cases from 24 to 31. There shouldn’t have a single error in any case, based on the correct truth table.

Complete in the "VHDL Code" cell, the code text (not image) in structural form (without errors) in VHDL syntax to turn on each of the values ​​of the common anode alphanumeric display as requested, respecting the name of inputs A, B, C, D and E, as well as outputs sA1, sA2, sB, sC, sD1, sD2, sE, sF, sG1, sG2, sH, sJ, sK, sL, sM and sN.

Physically implements the system on the FPGA board using the GPIO and the 16-segment display.